

M.C.A. EXAMINATION

May 2000
MCA 207
Second Semester)

COMPUTER ORGANIZATION AND
ARCHITECTURE

Time : 3 Hours

Maximum Marks : 80

Note : Attempt any *five* questions. All questions carry equal marks.

1. (a) Differentiate between Instruction Cycle and Execution Cycle. 4
- (b) A digital computer has a memory unit with a capacity of 8192 words, 36 bits per word. The instruction code format consists of 5 bits for the operation part and 13 bits for the address part (on indirect mode bit). Two instructions are packed in one memory word and a 36 bit instruction register IR is available in the control unit. Formulate the Fetch and Execution cycles for the computer. 12
- 2 (a) What is the difference between an immediate, a direct and an indirect address instruction? how many references to memory are needed for each (122)

$$235/005 = \frac{1}{4}$$

~~Type of instruction register~~
processor register?

(b) List the micro operations that of register A to bits 9-16 of re 1-8 of register B to bits 9-1 Draw a block diagram of the h

3 (a) Discuss the implementation programmed Calculator.

(b) Define the following terms in y

(i) Control memory

(ii) Hard-wired Control

(iii) Dynamic Programming

(iv) Control Word

(v) Micro Instruction

(vi) Micro Program

(vii) Micro-Code

(viii) Micro Operation

(ix) Micro Operation.

4. (a) Differentiate between RISC and C

(123)

$$235/005 = \frac{2}{4}$$

- (b) Derive an algorithm in flow chart form for the addition and subtraction of fixed point binary numbers in signed-magnitude representation with subtraction done by a parallel subtractor ($EA \leftarrow A - B$). Show one stage of the adder-subtractor circuit with an add-subtract control (ASC). 12
5. (a) What do you mean by Virtual Memory? 4
- (b) Explain the need for memory hierarchy. What is the main reason for not having a large enough main memory for storing the totality of information in a Computer System? 12
6. A digital computer has a memory unit of $64K \times 16$ and a cache memory of 1 K words. The cache use direct mapping with a block size of four words.
- (i) How many bits are there in the tag, index, block and word fields of the address format? 8
- (ii) How many bits are there in each word of cache and how are they divided into functions? Include a valid bit. 5
- (iii) How many blocks can the cache accommodate?

(124)

$$235/005 = 3 \frac{1}{1}$$

- (b) Explain the four types of commands that peripheral interface may receive when it addressed by the CPU. 8

Write short notes on any *four* of the following.

4 each

- (i) Instruction Set Selection
- (ii) Superscalar Processor
- (iii) Pipelining
- (iv) Memory Array Organizaion
- (v) SPEC-Marks

$$235/005 = \frac{4}{4}$$